HIGH-SPEED BUS WITH EMBEDDED CLOCK SIGNALS

ABSTRACT

A system and method for embedding at least one clock signal into bus lines that also carry data signals at other times to enable a high-speed bus is disclosed. Each bus line is used for carrying both clock and data information at different times. Data signals, which may be either encoded or not, are carried through a subset of the bus lines through a mapping scheme that maps the data information to the bus lines at each data transfer while the clock signals are carried in the remaining bus lines. Various mapping schemes are possible.